

## REMARKS

Claims pending in the present patent application are numbered 1-5 and 8-19. Claims 6 and 7 are canceled herein without prejudice. Claims 1-4, 8-10 and 13 are amended herein. No new matter has been introduced as a result of these amendments. The rejections set forth in the Office Action dated September 7, 2005, have been carefully considered by the Applicant. Applicant respectfully asserts that Claims 1-5 and 8-19 are in condition for allowance, and requests consideration of these claims.

## SPECIFICATION

The specification is amended herein to correct the informalities cited by the Examiner in the present Office Action. Applicant respectfully asserts that the specification is now in condition for allowance.

## CLAIM OBJECTIONS

Claim 1, 8 and 13 are amended herein to correct the informalities cited by the Examiner in the present Office Action.

## CLAIM REJECTIONS

### **35 USC § 102**

Claims 1-3, 8-10 and 13-16 are rejected under 35 U.S.C. 102 (b) as being anticipated by Wu (U.S. Publication 2002/0102793, hereinafter "Wu").

Claim 1 recites:

A method for fabricating a memory device comprising:  
depositing a first dopant in a first region of a semiconductor substrate of said memory device;  
subsequent to said depositing said first dopant, performing a first annealing process upon said semiconductor substrate, wherein said first annealing process diffuses said first dopant a pre-determined percentage of a first complete diffusion state;

subsequent to said performing said first annealing process, depositing a second dopant in a second region of said semiconductor substrate; and subsequent to said depositing said second dopant, performing a second annealing process upon said semiconductor substrate, wherein said second annealing process diffuses said first dopant to said first complete diffusion state and said second dopant to a second complete diffusion state.

Independent Claims 8 and 13 recite alternative embodiments of the invention recited in Claim 1. Claims 8 and 13 include a first annealing (or diffusion process, in Claim 13) after a first implant in a first region, a second depositing of a second dopant in a second region after the first annealing, and a second annealing (or diffusion process, in Claim 13) after the second dopant is deposited.

Wu teaches “a method of fabricating a shallow-trench-isolation (STI) structure for the channel width of [a] stacked-gate flash memory device array” ([0020]). Wu does not teach or suggest depositing a first dopant, performing a first annealing process after depositing the first dopant, depositing a second dopant after the first annealing process, then performing a second annealing process after depositing the second dopant, as recited in Claims 1, 8 and 13. In contrast, in paragraph [0026], referring to Figure 4F, Wu teaches a first implant of dopants into well **21b**, followed by an second implant of dopants into well **21c**, followed by a third implant into well **21a**. Wu does not teach or suggest any annealing processes being performed between any of these implants.

In later steps in the fabrication process, discussed in paragraph [0028], Wu teaches implanting impurities to form heavily doped source and common buried-source diffusion regions **40a**, as shown in Figure 5A. Continuing on to paragraph [0029], the implant into region **40a** is followed by a subsequent implant of boron impurities into regions **21b**, followed by implanting arsenic impurities into regions

**21c.** Wu does not teach or suggest any annealing processes occurring between any of these implants.

Wu does discuss annealing, later in paragraph [0029], for activating the implanted regions and to eliminate implant-induced defects. However, Wu teaches a singular annealing process for this purpose, and it does not occur between a first and second implant, as recited in Claims 1, 8 and 13. Wu also teaches a thermal annealing, in paragraph [0030], to form a titanium-disilicide layer, but Wu does not teach or suggest that this annealing process occurs between a first and second implant, as recited in Claims 1, 8 and 13.

Applicant respectfully traverses Examiner's rejection of Claims 1, 8 and 13 under 35 U.S.C. 102 (b) as being anticipated by Wu for the reasons above. Claims 2 and 3 depend on Claim 1 and recite additional limitations. Claims 9 and 10 depend on Claim 8 and recite additional limitations. Claims 14-16 depend on Claim 13 and recite additional limitations. Applicant respectfully traverses Examiner's rejection of Claims 2, 3, 9, 10 and 14-16 as being anticipated by Wu. Applicants respectfully assert that Claims 1-3, 8-10 and 13-16 are in condition for allowance.

### **35 USC § 103**

Claims 5-7, 11-12 and 17-19 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Wu. For the reasons discussed above, Applicant asserts that Independent Claims 1, 8 and 13 are in condition for allowance. Furthermore, there is no motivation in Wu to insert an annealing process between implant steps in Wu's fabrication process, as recited in Claims 1, 8 and 13.

Claims 6 and 7 are canceled herein without prejudice. Claim 5 is dependent on Claim 1 and recites an additional limitation. Claims 11-12 are dependent on Claim 8 and recite additional limitations. Claims 17-19 are dependent on Claim 13 and recite additional limitations. Therefore, Applicant respectfully traverses Examiner's rejection of Claims 5, 11-12 and 17-19 under U.S.C. (a) as being unpatentable over Wu. Applicant respectfully asserts that Claims 5, 11-12 and 17-19 are in condition for allowance.

### CONCLUSION

In light of the response presented herein, Applicants respectfully assert that Claims 1-5 and 8-19 overcome the rejection of record, and therefore earnestly solicit allowance of these claims.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,  
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